UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/016,346	12/10/2001	Charles Edward Kuhlmann	RPS920010125US1	6492

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EXAMINER
SIEK, VUTHE

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

	Application No.	Applicant(s)
Office Action Summary	10/016,346	KUHLMANN ET AL.
	Examiner	**Art Unit**
	Vuthe Siek	2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13* is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____ .

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

    a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). *2* .

4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: .

DETAILED ACTION

1. This office action is in response to application 10/016,346 filed on 12/10/2001.

Claims 1-13 remain pending in the application.

Specification

2. The disclosure is objected to because of the following informalities: related

applications information is missing (pages 1-2).

Appropriate correction is required.

Claim Objections

3. Claim 6 is objected to because of the following informalities: Claim 6 should depend

on claim 5 in order to result antecedent basis problem. Appropriate correction is

required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form

the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 4 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by

Calvignac et al. (US2002/0122386 A1).

6. As to claim 1, Calvignac et al. disclose high speed network processor comprising a

plurality of standard cells (for example data storage memory) ; at least one field

programmable gate array (FPGA) cell (Fig. 1, FPGA) that can communicate with at

least one of standard cells, wherein the FPGA cell allows for customization of the

network processor (FPGA is programmable) (Figs. 1-4)

7. As to claims 2-3, 4 and 7, remarks set forth in claim 1 equally apply here in rejecting

claims 4 and 7. In addition, Calvignac et al. teach wherein the at least one FPGA cell

can provide a specific function based upon field programming techniques to allow for

customization of the network processor (FPGA is programmable device); wherein the

standard cells are utilized for common logic and the at least one FPGA cell is utilized for

high risk logic (FPGA is programmable).

8. Claims 1-12 are rejected under 35 U.S.C. 102(a) as being anticipated by Product

Review from Adaptive Silicon Inc. (ASi), "Adaptive Silicon Announces FPGA Core,

March 12, 2001, pages 1-4.

9. As to claims 1-8, ASi discloses a customizable network processor comprising

embedded programmable logic core within ASIC and ASSP in a single silicon die. The

first embedded programmable logic core will enable ASIC and ASSP manufacturers to

add the flexibility and reduce the engineering costs of FPGAs to their products said

CEO of ASi. The embedded programmable logic core permits the high-risk blocks (high-

risk logic) of an SoC device to be modified after first silicon is produced. Consequently,

such devices may be fabricated earlier in the development process without risking

modification to the overall design or re-spinning the silicon. The embedded

programmable logic core also provides the flexibility to modify devices once they are

shipped to customers. As a result, algorithms can be upgraded and changes in

standards or protocols can be accommodated in applications like communications and

image processing. By architecting a family of products with embedded programmable

logic, it is possible to produce a number of different silicon products from single die,

avoiding the increasing costs of masks, prototype silicon and parallel engineering

development efforts. For design like networking products and wireless base station

applications, which are marked by evolving standards, embedded programmable logic

allows the design to be completed and the silicon built while changes are being made.

Changes are possible right up until product is finally released to customers. For

applications like network processor chip, where custom processors are often

implemented, co-processor or instruction-level functions can be implemented to

complement the primary processor functions. Thus, ASi introduces a network

processor comprising hybrid of FPGAs and ASICs or in standard products. It is noted

that custom logic file including a verification module to verify customized network

processor, and custom logic bill are inherently within a customable network processor

introduced by ASi comprising embedded programmable logic (FPGA) that permits high-

risk blocks (high-risk logic) on an SoC device to be modified after first silicon is

produced or in the process to produce. Since changes are possible right up until the

product (customized network processor) is finally released to customers, the network

processor is verified accordingly based on custom logic file or custom request.

10.   As to claims 9-12, since ASi introduces a customized network processor, said

customized network processor inherently includes a processor local bus (PLB), two on-

chip peripheral buses (OPBs), an accelerator function and a PLB master/slave function

for internal and external communications and in order to customize network processor

according to customer need.

11.   Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Craig

Matsumoto, "Lucent hybrid combines FPGA, ASIC features," EE times, August 18,

2000, page 1.

12.   As to claims 1-12, Matsumoto describes that Lucent discloses hybrid FPGA and

standard-cell ASIC features for a networking communications application including a

network processor. Since FPGA is programmable, thus the FPGA cell allows for

customization for the network processor. Matsumoto describes that programmable-

logic is added to the chips including FPGAs and ASICs. Since FPGAs are

programmable, the FPGAs provide a specific function based upon field programming

techniques to allow for customization of the network processor, and the plurality of

standard cells are utilized for common logic and the at least one FPGA cell is utilized for

high risk logic because the added FPGA would customize the network processor

according to customer need. Accordingly a custom logic file including a verification

module is inherently included within hybrid of FPGAs and standard-cell ASICs forming a

network processor, since adding FPGA would require verification in order to meet

design requirements. It is noted that a processor local bus (PLB), two on-chip

peripheral buses (OPBs), an accelerator function and a PLB master/slave function are

inherently included within the hybrid FPGAs and standard-cell ASICs of a network

processor chip.

13.   Claims 1-12 are rejected under 35 U.S.C. 102(a) as being anticipated by Mason

et al. (6,272,451).

14.   As to claims 1-12, Mason et al. teach a field-programmable-system-level

integrated circuit (FPSLIC) that can used as a network processor (Figs. 1A-1B), col. 1,

summary, col. 5, line 65 to col. 12, line 25) comprising a plurality of standard cells

(standard-cell ASIC and ASSP, col. 6); a plurality of FPGAs cells, wherein the FPGAs

allow customization of the network processor. The network processor comprising

FPSLIC architecture is ideal for implementation of networking, telecommunications,

multimedia, audio, handled, portable, and industrial control applications (col. 6). Thus,

the FPGAs allow for customization of the network processor to be suitable for such

above applications. Accordingly, the standard-cell ASIC and ASSP are utilized for

common logic and at one of the FPGAs is utilized for high risk logic, since FPGAs can

be embedded in FPSLIC chip designed to be suitable for an application. Since, the

FPGA core is embedded within FPSLIC chip that can be used for an application

(customer need), the FPSLIC is designed by providing a custom logic file with a

verification module in order to verify a complete FPSLIC design or a complete network

processor. Since, the FPSLIC chip (network processor) is designed for these above

applications, said FPSLIC chip would comprise a processor local bus (PLB), two on-

chip peripheral buses (OPBs), an accelerator function and a PLB master/slave function

(col. 5-col. 11).

Allowable Subject Matter

15.   Claim 13 is allowed over the prior art of record since the prior art does not

disclose a network processor as recited in the claim.

Conclusion

16.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Vuthe Siek whose telephone number is (703) 305-4958.

The examiner can normally be reached on M-F (6:30-4:00) 2nd Friday off.

        If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Matthew Smith can be reached on (703) 308-1323. The fax phone numbers

for the organization where this application or proceeding is assigned are (703) 872-9318

for regular communications and (703) 872-9319 for After Final communications.

        Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to the receptionist whose telephone number is (703) 308-

1782.

Vuthe Siek
Primary Examiner
June 16, 2003

VUTHE SIEK
PRIMARY EXAMINER